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Application Number	10/788,468
Filing Date	March 1, 2004
First Named Inventor	Junichi YANAGIHARA
Group Art Unit	2816
Examiner Name	Kenneth B. Wells
Total Number of Pages in This Submission	Attorney Docket Number: 031948-9

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
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Firm or Individual name	Luan C. Do, Reg. No. 38,434 Nixon Peabody LLP 401 9th Street, N.W. Suite 900 Washington, D.C. 20004-2128
Signature	
Date	October 2, 2006

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Michelle Duvall
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☐ Applicant claims small entity status. See 37 CFR 1.27

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Complete if Known	
Application Number	10/788,468
Filing Date	03/01/2004
First Named Inventor	Junichi YANAGIHARA
Examiner Name	Kenneth B. Wells
Art Unit	2816
Attorney Docket No.	031948-9

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FEE CALCULATION

1. BASIC FILING FEE

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1001	300	2001	150	Utility filing fee	
1002	200	2002	100	Design filing fee	
1003	200	2003	100	Plant filing fee	
1004	300	2004	150	Reissue filing fee	
1005	200	2005	100	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims	Fee from below	Fee Paid
Total Claims	-20** =		X =	0
Independent Claims	-3** =		X =	0
Multiple Dependent			X =	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	** Reissue independent claims over original patent
1205	50	2205	25	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within 2nd month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	500	2452	250	Petition to revive – unavoidable	
1453	1,500	2453	750	Petition to revive – unintentional	
1501	1,400	2501	700	Utility issue fee (or reissue)	
1502	800	2502	400	Design issue fee	
1503	1,100	2503	550	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
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October 2, 2006
Date

Michelle Duvall
Signature

Michelle Duvall
Typed or printed name

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	Luan C. Do	Registration No. *(Attorney/Agent)*	38,434	Telephone	(202) 585-8000
Signature				Date	October 2, 2006

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Docket No.: 031948-9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Patent Application of	)	Confirmation No.: 9233
Junichi YANAGIHARA	)	
Serial No. 10/788,468	)	Examiner: Wells, Kenneth B.
Filed: March 1, 2004	)	Art Unit: 2816
For: DIFFERENTIAL CURRENT DRIVER	)	
WITH SHUNTING ELEMENT (As Amended)	)	Date: **October 2, 2006**

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
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Michelle Duvall

Sir:

In accordance with the provisions of 35 U.S.C. §134 and 37 C.F.R. §41.37, Appellant submits this Appeal Brief in triplicate in support of the Notice of Appeal filed August 1, 2006, to appeal the Examiner's final rejections in the Final Office Action of March 1, 2006 and the Advisory Action mailed July 21, 2006.

I. REAL PARTY IN INTEREST

Oki Electric Industry Co., Ltd. is the assignee and real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences known to the Appellant, the Appellant's representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

For the purposes of this Appeal, claims 1-3, 21-22, 25-28 and 30 have been rejected, claims 23-24, 29 and 31-32 stand objected as being dependent upon a rejected base claim,

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and claims 4-20 have been canceled. Thus, this Appeal is taken from the rejection of claims 1-3, 21-22, 25-28 and 30, as submitted in the Appendix herewith.

IV. STATUS OF AMENDMENTS

No amendments have been made to the claims subsequent to the final rejections stated in the final Office Action of March 1, 2006 and to the Advisory Action of July 21, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This Appeal is taken from claims 1-3 and 21-32 that are pending for consideration, of which claims 1 and 21 are independent.

With respect to claim 1, the present invention recited therein relates to differential current driver having two output terminals (e.g., DP, DM in Fig. 1), a common node (e.g., N in Fig. 1), a current source (e.g., 2 in Fig. 1) supplying a first current to the common node (N), two switches (e.g., 3 and 4 in Fig. 1) connected to the common node (e.g., N) and to the two output terminals (e.g., DP, DM), and a circuit (e.g., 6, 7, 8 and 9 in Fig. 1) for selectively closing the two switches (e.g., 3,4) according to data to be transmitted, the current source (e.g., 2) having a control terminal receiving a bias signal (e.g., BIAS in Fig. 1), the first current being controlled by the bias signal, the differential current driver comprising:

a comparison circuit (e.g., 10) for receiving the bias signal and mirroring the first current to obtain a second current (e.g., from 23 in Fig. 2), comparing the second current with a reference value (e.g., 20 in Fig. 2) and generating a control signal (e.g., OUT in Fig. 2) having a value responsive to a difference between the second current and the reference value; and

a current adjustment circuit (e.g., 11 in Fig. 1) connected to the common node (e.g., N) for diverting part of the first current (e.g., from 2 in Fig. 1) away from the switches (e.g., 3, 4) responsive to the control signal (e.g., OUT).

With respect to claim 2, the present invention recited therein relates to a differential current driver of claim 1, wherein the current adjustment circuit (e.g., 11 in Fig. 1) comprises a transistor for shunting part of the first current to a node (e.g., ground) different from the two output terminals (e.g., DP, DM) and the common node (e.g., N).

With respect to claim 3, the present invention recited therein relates to a differential current driver of claim 2, wherein the node different from the two output terminals and the

common node is a ground node, and the transistor has a source terminal connected to the ground node, a gate terminal receiving the control signal, and a drain terminal connected to the common node.

With respect to claim 21, the present invention recited therein relates to a differential current driver comprising:

a first transistor (e.g., 2 in Fig. 1) connected to a first node (e.g., N in Fig. 1), the first transistor (e.g., 2) having a gate electrode connected to a second node (e.g., BIAS input or gate of transistor 2 in Fig. 1);

a first switch circuit (e.g., 3 in Fig. 1) connected to the first node (N) and a first output terminal (e.g., DP in Fig. 1);

a second switch circuit (e.g., 4 in Fig. 1) connected to the first node (N) and a second output terminal (e.g., DM in Fig. 1);

a controller (e.g., 6, 7, 8 and 9 in Fig. 1) controlling the first (e.g., 3) and second (e.g., 4) switch circuits according to voltage levels of two input signals (e.g., DATA and OE in Fig. 1);

a comparison circuit (e.g., 10) connected to the second node, for comparing a first current (e.g., from current source 2 in Fig. 1) generated by a voltage level of the second node and a reference current (e.g., from reference current source 20 in Fig. 2) and outputting a comparison result (e.g., OUT in Figs. 1 and 2); and

an adjustment circuit (e.g., 11 in Fig. 1) generating a current path between the first node (e.g., N) and ground on the basis of the comparison result.

With respect to claim 22, the present invention recited therein relates to a differential current driver of claim 21, wherein the first transistor (e.g., 2 in Fig. 1) is a p-channel metal-oxide-semiconductor (PMOS) transistor.

With respect to claim 23, the present invention recited therein relates to a differential current driver of claim 22, wherein the first (e.g., 3 in Fig. 1) and second (e.g., 4 in Fig. 1) switch circuits are PMOS transistors.

With respect to claim 24, the present invention recited therein relates to a differential current driver of claim 22, wherein the adjustment circuit (e.g., 11 in Fig. 1) is a PMOS transistor.

With respect to claim 25, the present invention recited therein relates to a differential current driver of claim 21, wherein the comparison circuit comprises:

a second transistor (e.g., 23 in Fig. 2) having a gate electrode connected to the second node;

a reference current source (e.g., 20 in Fig. 2) generating the reference current; and

a differential amplifier (e.g., 24 in Fig. 2) connected to the second transistor (e.g., 23) and the reference current source (e.g., 20) and outputting the comparison result (e.g. OUT).

With respect to claim 26, the present invention recited therein relates to a differential current driver of claim 25, wherein the second transistor is proportional to the first transistor, as supported in the second full paragraph on page 9 of the original specification.

With respect to claim 27, the present invention recited therein relates to a differential current driver of claim 26, wherein a drain current of the second transistor is smaller than a drain current of the first transistor, as supported in the second full paragraph on page 9 and in the first full paragraph on page 11 of the original specification.

With respect to claim 28, the present invention recited therein relates to a differential current driver of claim 27, wherein the second transistor is a PMOS transistor.

With respect to claim 29, the present invention recited therein relates to a differential current driver of claim 25 wherein the comparison circuit further comprises a current mirror circuit connected to the second transistor and the reference current source.

With respect to claim 30, the present invention recited therein relates to a differential current driver of claim 21, wherein the controller comprises:

a first inverter (e.g., 6 in Fig. 1) receiving a first signal (e.g., DATA);

a second inverter (e.g., 7 in Fig. 1) connected to the first inverter;

a first NAND (e.g., 8 in Fig. 1) circuit connected to the second inverter and the first switch circuit (e.g., 3 in Fig. 1) and receiving a second signal (e.g., OE); and

a second NAND circuit (e.g., 9 in Fig. 1) connected to the first inverter and the second switch circuit (e.g., 4 in Fig. 1) and receiving the second signal (e.g., OE).

With respect to claim 31, the present invention recited therein relates to a differential current driver of claim 30, wherein the first (e.g., 3 in Fig. 1) and second (e.g., 4 in Fig. 1) switch circuits are PMOS transistors.

With respect to claim 32, the present invention recited therein relates to a differential current driver of claim 31, wherein the first NAND circuit (e.g., 8 in Fig. 1) is connected to a

gate electrode of the first switch circuit (e.g., 3 in Fig. 1), and the second NAND circuit (e.g., 9 in Fig. 1) is connected to a gate electrode of the second switch circuit (e.g., 4 in Fig. 1).

According to, e.g., page 3 of the specification, the present invention as recited in the independent claims summarized above prevents an output of excess of current at a transition from an output-disable state to an output-enable state of a differential current driver without significantly increasing the current consumption of the differential current driver. Further, the present claimed invention allows data transmission by a differential current driver at high speed with low power consumption.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The ground of rejection to be reviewed on appeal is the rejection of claims 1-3, 21-22 and 25-28 under 35 U.S.C. §102(b) as being anticipated by Altmann (U.S. Patent No. 6,448,848 – hereafter Altmann).

B. The ground of rejection to be reviewed on appeal is the rejection of claim 30 under 35 U.S.C. §103(a) as unpatentable over Altmann.

ARGUMENTS

A. In the Final Office Action of March 1, 2006, the Examiner asserts that claims 1-3, 21-22 and 25-28 are anticipated by Altmann the Examiner equates Appellant's common node (i.e., node N in Appellant's Fig. 1) to the common sources of NMOS FETs M_1 and M_2 in g_m cell 110 in Altmann's Fig. 1. The Examiner further equates Appellant's recited current source to one or both of the PMOS FETs 115 of Altmann. Specifically, on page 2, lines 9-10 of the Final Office Action, the Examiner stated, *"...the cited current source is either or both of the FETs 115"*. Still further, the Examiner equates Appellant's claimed comparison circuit to the combination of g_m cell 120 and amplifier A(s) of Altmann. These assertions are improper for the following reasons.

Initially, Appellant respectfully notes that in the Advisory Action mailed July 21, 2006, the Examiner denied that he ever asserted that FETs 115 as equivalent to Appellant's claimed current source. However, as quoted above, the Examiner clearly made the assertion that Appellant's cited current source is either or both of the FETs 115 of Altmann.

Further, in the Advisory Action the Examiner alleged that Appellant's improperly argued the differences between the prior art and the disclosed invention and not the claimed invention. However, such an allegation is completely insupportable because each of the limitations compared and discussed in relation to the disclosed features of Altmann are recited in Appellant's pending claims.

Still further, in the Advisory Action, the Examiner stated "... as well known in the art of semiconductor IC technology, any element that sources a current can be considered to be a current source (especially using the broadest reasonable interpretation test)." In response, Appellant understands that such a statement is an Official Notice and respectfully requests the Examiner to provide proper support in accordance to MPEP 2144.03. Moreover, Appellant submits herewith the Memorandum from the Deputy Commissioner for Patent Examination Policy, Steve Kunin, which is titled *Procedures for Relying on Facts Which are Not of Record as Common Knowledge or for Taking Official Notice,* for the Examiner's reference.

Still further, with respect to the "broadest reasonable test" that the Examiner has applied, Appellant respectfully requests the Examiner to provide proper authority to explain and support the "test" that the Examiner alluded to. Moreover, Appellant respectfully submits that claim language should be read in light of the specification. Further, in asserting equivalence, the Examiner should take the following points into consideration:

> *1) Whether the prior art element performs the function specified in the claim in substantially the same way, and produces substantially the same results as the corresponding element disclosed in the specification.*
>
> *2) Whether a person of ordinary skill in the art would have recognized the interchangeability of the element shown in the prior art for the corresponding element disclosed in the specification.*
>
> *3) Whether the prior art element is a structural equivalent of the corresponding element disclosed in the specification being examined. That is, the prior art element performs the function specified in the claim in substantially the same manner as the function is performed by the corresponding element described in the specification.*

If the FETs 115 were equivalent to Appellant's claimed current source, then Altmann would appear to have two current sources connected in gm-C cell 110, as Appellant will explain in detail below. Hence, FETs 115 cannot be structurally and functionally equivalent to Appellant's claimed current source.

As submitted in the Request for Reconsideration filed July 3, 2006, Appellant will show again below that Altmann's circuits, when analyzed according to Altmann's teaching and to proper understanding circuit theory, do not correspond to Appellant's claimed features and do not perform the same functions as Appellant's claimed invention.

In order to facilitate the comparison of Appellant's claimed invention with that of Altmann, Appellant attaches herewith a marked-up Fig. 1 of Altmann and two pages of publication directed to Thevenin's, Norton's, and Maximum Power Transfer Theorems, specifically to ideal current sources.

Referring to Altmann's Fig. 1, Appellant notes current I_1 flowing from a supply line at the top of the drawing to a current source line at the bottom of the drawing. This bottom line is identified indirectly as the current source line in Col. 2, lines 42-46 of Altmann because it is the line to which capacitors C_1 and C_2 are tied. The current source line is connected to ground, as denoted by the ground symbol in Fig. 1. Since M_1 and M_2 are NMOS transistors (see Col. 2, lines 27-28 of Altmann), their common sources must be the on the ground side, and the common node must therefore be the point at which M_1 and M_2 are connected to the circuit element indicated by two intersecting circles, which is connected to the source line. This pair of intersecting circles, although not explicitly identified by Altmann, would be understood by a person skilled in the art to indicate a current source, a circuit that (ideally) outputs a constant current regardless of the load imposed on it.

At this point, Appellant would like to point the Examiner's attention to the attached publication regarding Thevenin's, Norton's, and Maximum Power Transfer Theorems which defines "ideal current source" and shows the symbol representing ideal current source as two intersecting circles; and, incidentally, Appellant notes that this circuit element (i.e., the current source denoted by the two intersecting circles) of Altmann is most closely identified with Appellant' current source recited in claim 1, and that the Examiner's assertion that either or both of FETs 115 is equivalent to Appellant's claimed current source is insupportable.

As summarized above, in the rejection, the Examiner asserts that the PMOS transistor 115 are equivalent to Appellant's claimed current source. However, Appellant respectfully asserts that the PMOS transistors 115 of Altmann cannot be identified as an equivalence of Appellant's claimed current source because the PMOS transistors 115 are connected to the drains, not the sources, of the NMOS transistors M_1 and M_2, and therefore are not connected to the "common node" as alleged by the Examiner.

Moreover, Appellant respectfully asserts that one skilled in the art would also recognize the pair of PMOS transistors 115 in Altmann's Fig. 1 as load elements, not a current source, that conduct varying currents ($I_1/2 + I_3$ and $I_1/2 + I_4$, or $I_1 + I_3 + I_4$ in total) that depend in part on the control signal supplied by amplifier A(s) to transistors M_3 and M_4.

With respect to the comparison circuit recited in claim 1, Appellant respectfully asserts that the claimed comparison circuit receives the same bias signal as the current source and mirrors the current supplied by the current source to the common node. However, in Altmann's Fig. 1, although it appears that the PMOS transistors in g_m cell 120 receive the same bias signal as the PMOS transistors 115 in g_m cell 110, this does not imply that the PMOS transistors mirror any of the currents ($I_1/2 + I_3$, $I_1/2 + I_4$, or $I_1 + I_3 + I_4$) conducted by the PMOS transistors 115 singly or in combination. The reason is that while the PMOS transistors 115 in g_m cell 110 carry both a constant current I_1 flowing toward the bottom of the cell and variable currents (I_3 and I_4) flowing out from the cell, the PMOS transistors in g_m cell 120 carry only the constant current I_1. Accordingly, g_m cell 120 and amplifier A(s) do not correspond to Appellant's comparison circuit recited in claim 1.

The Examiner's assertion that the NMOS transistors M_1 and M_2 in Altmann's Fig. 1 are equivalent to Appellant's switches is also improper. When Fig. 1 is interpreted in relation to the discussion in Col. 1, lines 13-32 of Altmann, it becomes clear to the skilled artisan that transistors M_1 and M_2 function as amplifying elements rather than switching elements.

With respect to the anticipatory rejection of independent claim 21 and its respective dependent claim, the arguments set forth above in relation to the rejection of claim 1 are also applicable. In comparison of Appellant's claim 1 and claim 21, the common node of claim 1 is recited as a first node in claim 21, the current source is recited as a first transistor, and its bias signal is recited as the voltage at a second node. In addition to the arguments set forth above, Appellant would like to add the following remarks with respect to claim 21.

The comparison circuit recited in claim 21 compares a current generated from the second node voltage with a reference current. On the other hand, in Altmann's g_m cell 120, the constant current I_1 output by the current source denoted by intersecting circles is forced through a varying resistance (i.e., the resistance offered by the NMOS transistors varies according to the signals out and outb supplied to their gate electrodes) and the resulting variable voltage is compared with a reference voltage (i.e., CM ref). Although Altmann does not specifically state that 'CM ref' is a voltage, the use of the terms 'CM voltage' and 'CM reference' in claims 1 and 2 of Altmann implies that CM ref in Fig. 1 is a voltage.

Accordingly, while Appellant's comparison circuit recited in claim 21 compares a variable current with a reference current, Altmann's g_m cell 120 and amplifier A(s) compare a variable voltage generated from a constant current and variable resistance with a reference voltage. Hence, the comparison circuit of the presently claimed invention differs from Altmann's g_m cell 120 and amplifier A(s).

Further, as submitted in the Amendment filed January 9, 2006, the present invention is a feed-forward circuit while Altmann's is a feedback circuit, as disclosed in Col. 2, lines 50-52, claims 1-3, claims 5-7, etc. Although Appellant is not claiming a feed-forward circuit explicitly, Appellant would like to point out the distinctions between Appellant's feed-forward circuit and Altmann's feedback circuit in order to show that the cooperative parts of the invention of Altmann are different structurally and also functionally, and that the assertions of equivalence made by the Examiner are not proper because, when taken as a whole or by each individual limitation, Appellant's claimed invention is different structurally and functionally than Altmann's.

Moreover, the purpose of the circuit set forth in accordance with Appellant's claimed invention is to suppress sudden high current output on one of two output signal lines when the output changes from the disabled to the enabled state, while the purpose of Altmann's circuit is to control common-mode output current on both output signal lines during continuous operation of the circuit.

As noted above, Appellant's claimed comparison circuit receives the bias signal or second node voltage signal (as recited in claim 21), while Altmann's comparison circuit A(s) instead receives a common mode voltage generated from the outputs of M_1 and M_2.

Additionally, the adjustment circuit set forth in accordance with Appellant's claimed invention is connected to the common node (e.g., N) as recited in independent claim 1, or first node as recited in independent claim 21, while Altmann's transistors M_3 and M_4 are connected to the output terminals, specifically out and outb.

It is noted that at least the differences discussed above cause Appellant's circuit and Altmann's circuit to operate in completely different manners. That is, the present circuit as recited in Appellant's claimed invention responds to the amount of current supplied by the constant-current source, which changes temporarily when the output changes from the disabled state (both switches off) to the enabled state (one switch on, on switch off). On the other hand, Altmann's circuit responds to a voltage drop produced by an unchanging constant current conducted through a g_m cell (120) that receives varying outputs.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Altmann, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-3, 21, 22 and 25-28, under 35 U.S.C. §102(b), as anticipated by Altmann is improper.

B. In the rejection, the Examiner acknowledge that Altmann does not teach or disclose a specific type of driver circuit. The Examiner then stated "nevertheless [it] would have been obvious to one of ordinary skill in the art who will easily recognize that any type of differential driver can be used to supply Fig. 1 circuitry with its inputs..." Appellant respectfully contends that the Examiner has failed to set forth a *prima facie* case of obviousness for the following reasons:

The Supreme Court, in *Graham v. John Deere*, set forth the basic test for patentability under 35 U.S.C. §103.[1]

> Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unresolved need, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter to be patented.

Moreover, in *In re Ehrreich and Avery*, the Court of Customs and Patent Appeals further clarified the basic test set forth in *Graham v. John Deere*.[2]

> We must not here consider a reference in a vacuum, but against the background of the other references of record which may disprove theories and speculations in the reference or reveal previously undiscovered or unappreciated problems. The question in a §103 case is what the references would collectively suggest to one of ordinary skill in the art. *In re Simon*, 461 F.2d 1387, 174 USPQ 114 (CCPA 1972). It is only by proceeding in this manner that we may fairly determine the scope and content of the prior art according to the mandate of *Graham v. John Deere*, 383 US 1, 17, 148 USPQ 459, 467 (1966)(Emphasis in original.)

It should be noted that three criteria must be met to establish a *prima facie* case of obviousness.[3] First, there must be some teaching, suggestion or motivation to do so found

[1] See *Graham v. John Deere*, 383 U.S. 1 at 18, 148 USPQ 459 at 167 (1996)

[2] See *In re Ehrreich and Avery*, 200 USPQ 504, 509-510 (CCPA 1979)

either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.[4] Second, there must be a reasonable expectation of success.[5] Last, the prior art must teach or suggest all the claim limitations.[6]

With respect to the present application, Appellant contends that the Examiner has failed to set forth a *prima facie* case of obviousness. In particular, Altmann fails to teach, disclose or suggest all of the limitations recited in the claimed invention. Specifically, Altmann fails to teach, disclose or suggest a current source and a comparison circuit, for example, in combination with the remaining cited features of claim 30.

Further, Altmann fails to teach, disclose or suggest inverters (e.g., 6, 7) in combination with NAND gates (8, 9) and receiving a first signal (e.g., DATA) and a second signal (e.g., OE) input as recited in claim 30. Appellant respectfully requests the Examiner to provide proper evidence supporting his technically insupportable assertion that any type differential driver can be used to supply Fig. 1 circuitry with inputs, as asserted by the Examiner.

Moreover, Appellant respectfully submit that the DATA signal and the OE signal in the present invention need to follow a certain timing, such as shown in Fig. 3, for example, such that proper operation of the claimed circuit can function as designed. That is, the specifically claimed configuration of the claimed controller comprising inverters and NAND gates is necessary with the input signals to effect the proper operation with the rest of the claimed differential driver. Further, there is no suggestion or motivation for Altmann to have any specific timing constraints with input signals, such as DATA and OE inputs, in a controller.

(Footnote continued from previous page)

[3] See *M.P.E.P. §2143*

[4] See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

[5] See *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976)

[6] See *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Accordingly, for at least the reasons outlined above, Appellant respectfully submits that U.S. Patent No. 6,448,848 to Altmann fails to teach, suggest, or disclose, either expressly or inherently, the features of the claimed invention as recited in independent claims 1 and 21. Thus, Altmann cannot be applied to in the rejection of claim 30 to render the claimed invention obvious.

Respectfully submitted,

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VI. CLAIMS APPENDIX

1. (Previously Presented) A differential current driver having two output terminals, a common node, a current source supplying a first current to the common node, two switches connected to the common node and to the two output terminals, and a circuit for selectively closing the two switches according to data to be transmitted, the current source having a control terminal receiving a bias signal, the first current being controlled by the bias signal, the differential current driver comprising:

a comparison circuit for receiving the bias signal and mirroring the first current to obtain a second current, comparing the second current with a reference value and generating a control signal having a value responsive to a difference between the second current and the reference value; and

a current adjustment circuit connected to the common node for diverting part of the first current away from the switches responsive to the control signal.

2. (Previously Presented) The differential current driver of claim 1, wherein the current adjustment circuit comprises a transistor for shunting part of the first current to a node different from the two output terminals and the common node.

3. (Previously Presented) The differential current driver of claim 2, wherein the node different from the two output terminals and the common node is a ground node, and the transistor has a source terminal connected to the ground node, a gate terminal receiving the control signal, and a drain terminal connected to the common node.

4-20. (Canceled)

21. (Previously Presented) A differential current driver comprising:

a first transistor connected to a first node, the first transistor having a gate electrode connected to a second node;

a first switch circuit connected to the first node and a first output terminal;

a second switch circuit connected to the first node and a second output terminal;

a controller controlling the first and second switch circuits according to voltage levels of two input signals;

a comparison circuit connected to the second node, for comparing a first current generated by a voltage level of the second node and a reference current and outputting a comparison result; and

an adjustment circuit generating a current path between the first node and ground on the basis of the comparison result.

22. (Previously Presented) The differential current driver of claim 21, wherein the first transistor is a p-channel metal-oxide-semiconductor (PMOS) transistor.

23. (Previously Presented) The differential current driver of claim 22, wherein the first and second switch circuits are PMOS transistors.

24. (Previously Presented) The differential current driver of claim 22, wherein the adjustment circuit is a PMOS transistor.

25. (Previously Presented) The differential current driver of claim 21, wherein the comparison circuit comprises:

a second transistor having a gate electrode connected to the second node;

a reference current source generating the reference current; and

a differential amplifier connected to the second transistor and the reference current source and outputting the comparison result.

26. (Previously Presented) The differential current driver of claim 25, wherein the second transistor is proportional to the first transistor.

27. (Previously Presented) The differential current driver of claim 26, wherein a drain current of the second transistor is smaller than a drain current of the first transistor.

28. (Previously Presented) The differential current driver of claim 27, wherein the second transistor is a PMOS transistor.

29. (Previously Presented) The differential current driver of claim 25 wherein the comparison circuit further comprises a current mirror circuit connected to the second transistor and the reference current source.

30. (Previously Presented) The differential current driver of claim 21, wherein the controller comprises:

a first inverter receiving a first signal;

a second inverter connected to the first inverter;

a first NAND circuit connected to the second inverter and the first switch circuit and receiving a second signal; and

a second NAND circuit connected to the first inverter and the second switch circuit and receiving the second signal.

31. (Previously Presented) The differential current driver of claim 30, wherein the first and second switch circuits are PMOS transistors.

32. (Previously Presented) The differential current driver of claim 31, wherein the first NAND circuit is connected to a gate electrode of the first switch circuit, and the second NAND circuit is connected to a gate electrode of the second switch circuit.

VII. EVIDENCE APPENDIX

Attachment 1 – marked up Fig. 1 of Altmann (U.S. Patent No. 6,448,848)

Attachment 2 – definition of ideal current source

Steve Kunin, "*Procedures for Relying on Facts Which are Not of Record as Common Knowledge or for Taking Official Notice*"

VIII. RELATED PROCEEDINGS APPENDIX

There are no related proceedings to this Appeal.

ATTACHMENT 1

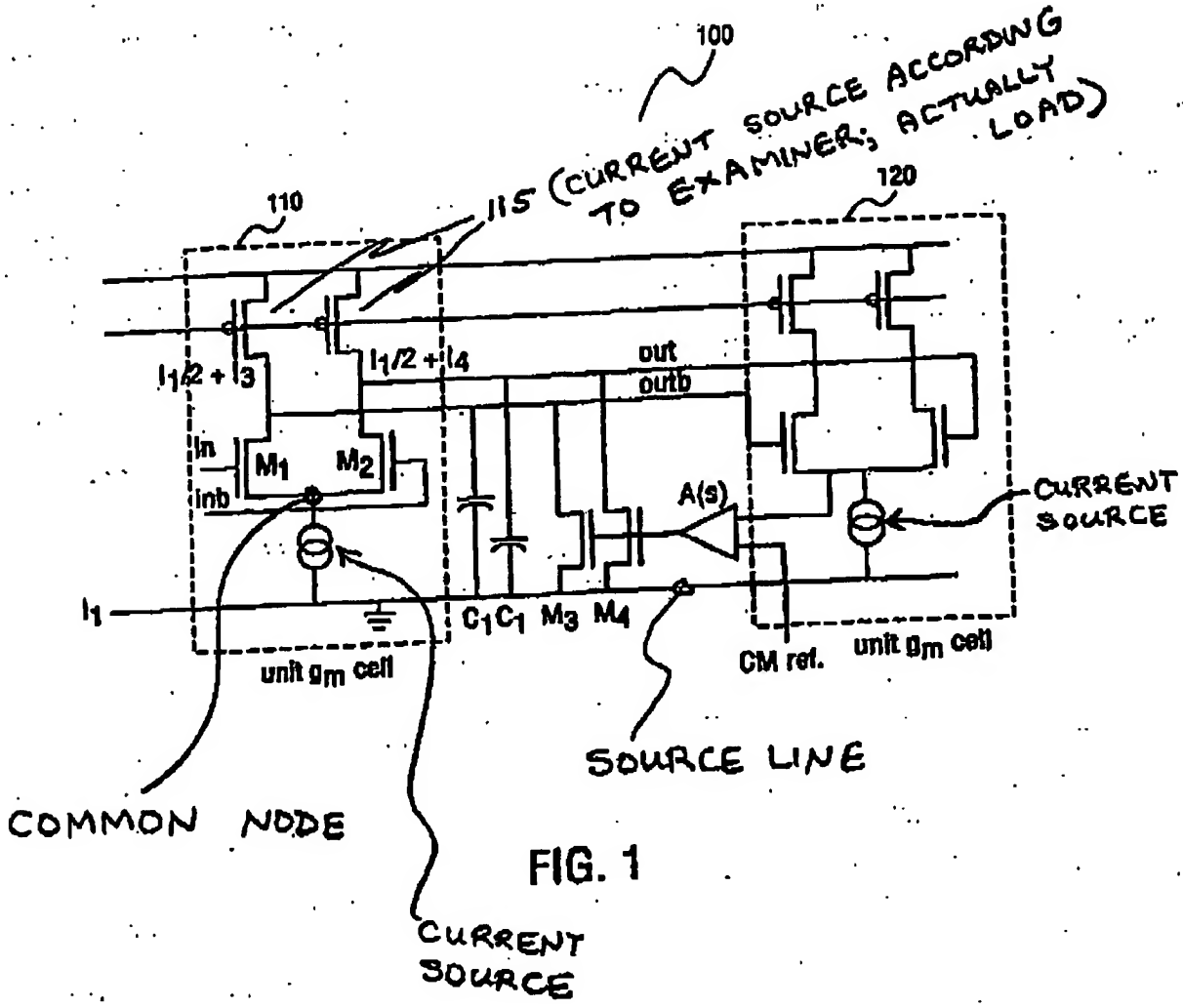


FIG. 1

http://www.biblio.org/obp/books/socratic/output/ (thev.pdf

Thévenin's, Norton's, and Maximum Power Transfer theorems

Resources and methods for learning about these subjects (list a few here, in preparation for your research):

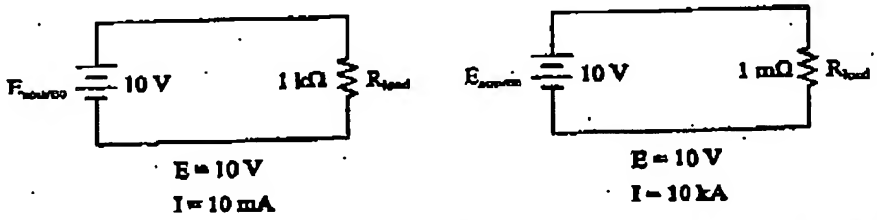
ATTACHMENT 2

ATTACHMENT 2

Question 2

A *voltage source* is a source of electricity that (ideally) outputs a constant voltage. That is, a perfect voltage source will hold its output voltage constant regardless of the load imposed upon it:

Ideal voltage sources assumed



E = 10 V
I = 10 mA

E = 10 V
I = 10 kA

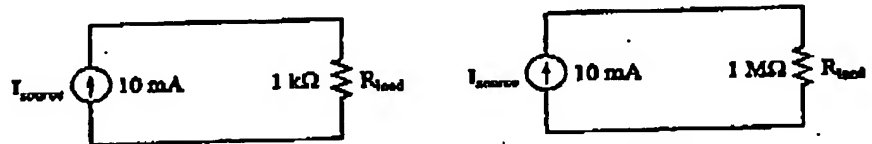
In real life, there is no such thing as a perfect voltage source, but sources having extremely low internal resistance come close.

Another type of electricity source is the *current source*, which (ideally) outputs a constant current regardless of the load imposed upon it. A common symbol for a current source is a circle with an arrow inside (always pointing in the direction of conventional flow, not electron flow!). Another symbol is two intersecting circles, with an arrow nearby pointing in the direction of conventional flow:

Current sources

Predict how an ideal current source would behave for the following two load scenarios:

Ideal current sources assumed



E = ???
I = 10 mA

E = ???
I = 10 mA

file 01735

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COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 2023
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Date: February 21, 2002

To: Patent Examining Corps
Technology Center Directors

From: Stephen G. Kunin
Deputy Commissioner for Patent Examination Policy

Subject: Procedures for Relying on Facts Which are Not of Record as Common Knowledge or for Taking Official Notice

This memorandum clarifies the circumstances in which it is appropriate to take official notice of facts not in the record or to rely on "common knowledge" in making a rejection.

Recent court decisions have affected the Office's practice of taking official notice of facts by relying on common knowledge in the art without a reference. Specifically, the Supreme Court recently changed the standard of review applied to decisions of the Board of Patent Appeals and Interferences and the Trademark Trial and Appeal Board on appeal to the U.S. Court of Appeals for the Federal Circuit. *Dickinson v. Zurko*, 527 U.S. 150, 50 USPQ2d 1930 (1999). As a result, the Federal Circuit now reviews findings of fact under the "substantial evidence" standard under the Administrative Procedure Act (APA), rather than the former "clearly erroneous" standard. *In re Gartside*, 203 F.3d 1305, 1315, 53 USPQ2d 1769, 1775 (Fed. Cir. 2000).[1] This change in the review standard has affected the Federal Circuit's view of when the court or the USPTO may take notice of facts without specific documentary evidence support.[2]

On remand from the Supreme Court, the Federal Circuit in *In re Zurko*, 258 F.3d 1379, 59 USPQ2d 1693 (Fed. Cir. 2001), reversed the Board's decision upholding a rejection under 35 U.S.C. 103 for lack of substantial evidence. Specifically, in *Zurko* and other recent decisions, the court criticized the USPTO's reliance on "basic knowledge" or "common sense" to support an obviousness rejection, where there was no evidentiary support in the record for such a finding.[3] In light of the recent Federal Circuit decisions and the substantial evidence standard of review now applied to USPTO Board decisions, the following guidance is provided in order to assist the examiners in determining when it is appropriate to take official notice of facts without

supporting documentary evidence or to rely on common knowledge in the art in making a rejection, and if such official notice is taken, what evidence is necessary to support the examiner's conclusion of common knowledge in the art.

(1) Determine when it is appropriate to take official notice without documentary evidence to support the examiner's conclusion.

Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances. While "official notice" may be relied on, as noted in MPEP § 2144.03, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known.[4] In appropriate circumstances, it might not be unreasonable to take official notice of the fact that it is desirable to make something faster, cheaper, better, or stronger without the specific support of documentary evidence. Furthermore, it might not be unreasonable for the examiner in a first Office action to take official notice of facts by asserting that certain limitations in a dependent claim are old and well known expedients in the art without the support of documentary evidence provided the facts so noticed are of notorious character and serve only to "fill in the gaps" which might exist in the evidentiary showing made by the examiner to support a particular ground of rejection.[5]

It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art.[6]

It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based.[7] As the court held in *Zurko*, an assessment of basic knowledge and common sense that is not based on any evidence in the record lacks substantial evidence support.[8]

(2) If official notice is taken of a fact, unsupported by documentary evidence, the technical line of reasoning underlying a decision to take such notice must be clear and unmistakable.

Ordinarily, there must be some form of evidence in the record to support an assertion of common knowledge.[9] In certain older cases, official notice has been taken of a fact that is asserted to be "common knowledge" without specific reliance on documentary evidence where the fact noticed was readily verifiable, such as when other references of record supported the noticed fact, or where there

was nothing of record to contradict it.[10] If such notice is taken, the basis for such reasoning must be set forth explicitly. The examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge.[11] The applicant should be presented with the explicit basis on which the examiner regards the matter as subject to official notice and be allowed to challenge the assertion in the next reply after the Office action in which the common knowledge statement was made.

(3) If applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the examiner must support the finding with adequate evidence.

To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art.[12] A general allegation that the claims define a patentable invention without any reference to the examiner's assertion of official notice would be inadequate. If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained.[13] If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 CFR 1.104(d)(2).

If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate. If the traverse was inadequate, the examiner should include an explanation as to why it was inadequate.

(4) Determine whether the next Office action should be made final.

If the examiner adds a reference in the next Office action after applicant's rebuttal, and the newly cited reference is added only as directly corresponding evidence to support the prior common knowledge finding, and it does not result in a new issue or constitute a new ground of rejection, the Office action may be made final. If no amendments are made to the claims, the examiner must not rely on any other teachings in the reference if the rejection is made final. If the newly cited reference is added for reasons other than to support the prior common knowledge statement and a new ground of rejection is introduced by the examiner that is not necessitated by applicant's amendment of the claims, the rejection may not be made final. See MPEP § 706.07(a).

(5) Summary.

Any rejection based on assertions that a fact is well-known or is common knowledge in the art without documentary evidence to support the examiner's conclusion should be judiciously applied. Furthermore, as noted by the court in *Ahlert*, any facts so noticed should be of notorious character and serve only to "fill in the gaps" in an insubstantial manner which might exist in the evidentiary showing made by the examiner to support a particular ground for rejection. It is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based.[14]

MPEP § 2144.03 will be revised accordingly in the upcoming revision to be consistent with this memo.

Cc: Nicholas Godici
Esther Kepplinger
Kay Kim
David Lacey

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[1] The Supreme Court has described substantial evidence review in the following manner:

> Substantial evidence is more than a mere scintilla. It means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion...Mere uncorroborated hearsay or rumor does not constitute substantial evidence.

Consolidated Edison Co. v. NLRB, 305 U.S. 197, 229-30 (1938)(quoted in *Gartside*, 203 F.3d at 1312, 53 USPQ2d at 1773). "'Substantial evidence' review involves examination of the record as a whole, taking into account evidence that both justifies and detracts from an agency's decision." *Gartside*, 203 F.3d at 1312, 53 USPQ2d at 1773 (citing *Universal Camera Corp. v. NLRB*, 340 U.S. 474, 487-88 (1951)). Furthermore, the Supreme Court has also recognized that "the possibility of drawing two inconsistent conclusions from the evidence does not prevent an administrative agency's finding from being supported by substantial evidence." *Consolo v. Federal Maritime Comm'n*, 383 U.S. 607, 620 (1966) (quoted in *Gartside*, 203 F.3d at 1312, 53 USPQ2d at 1773).

[2] See *Packard Press, Inc. v. Hewlett-Packard Co.*, 227 F.3d 1352, 1360, 56 USPQ2d 1351, 1356 (Fed. Cir. 2000) (questioning authority to take judicial notice for the first time on appeal in light of the APA standard of review established by *Dickinson v. Zurko*, 527 U.S. at165, 50 USPQ2d at 1937). Although the substantial evidence standard is deferential to the agency's decision, it imposes certain evidentiary requirements that must be met by the agency in formulating a decision. The Federal Circuit explained that "[i]n appeals from the Board, we have before us a comprehensive record that contains the arguments and evidence presented by the parties, including all of the relevant information upon which the board relied in rendering its decision." *Gartside*, 203 F.3d at 1314, 53 USPQ2d at 1774. Furthermore, the record is "closed, in that the Board's decision must be justified within the four corners of that record." *Id.* Thus, the record before the USPTO "dictates the parameters of review" available to the court. *Id.* Accordingly, "the Board's opinion must explicate its factual conclusions, enabling [the court] to verify readily whether those conclusions are indeed supported by 'substantial evidence' contained within the record." *Id.* (citing *Gechter v. Davidson*, 116 F.3d 1454, 1460, 43 USPQ2d 1030, 1035 (Fed. Cir. 1997)).

[3] *Zurko*, 258 F.3d at 1385, 59 USPQ2d 1697 ("the Board cannot simply reach conclusion based on its own understanding or experience—or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings."). See also *In re Lee*, __F.3d__, __, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002) (The Board determined that it was not necessary to present a source of a teaching, suggestion, or motivation to combine the references

because the conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art. The court reversed the Board's decision in sustaining a rejection under 35 U.S.C. 103 and stated that "'common knowledge and common sense' on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation...The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies").

[4] As noted by the court in *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970), the notice of facts beyond the record which may be taken by the examiner must be "capable of such instant and unquestionable demonstration as to defy dispute" (citing *In re Knapp Monarch Co.*, 296 F.2d 230, 132 USPQ 6 (CCPA 1961)). In *Ahlert*, the court held that the Board properly took judicial notice that "it is old to adjust intensity of a flame in accordance with the heat requirement." See also *In re Fox*, 471, F.2d 1405, 1407, 176 USPQ 340, 341 (CCPA 1973) (the court took "judicial notice of the fact that tape recorders commonly erase tape automatically when new 'audio information' is recorded on a tape which already has a recording on it").

[5] *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697; *In re Ahlert*, 424 F.2d at 1092, 165 USPQ at 421.

[6] *In re Ahlert*, 424 F.2d at 1091, 165 USPQ at 420-21. See also *In re Grose*, 592 F.2d 1161, 1167-68, 201 USPQ 57, 63 (CCPA 1979) ("[w]hen the PTO seeks to rely upon a chemical theory, in establishing a prima facie case of obviousness, it must provide evidentiary support for the existence and meaning of that theory."); *In re Eynde*, 480 F.2d 1364, 1370, 178 USPQ 470, 474 (CCPA 1973) ("we reject the notion that judicial or administrative notice may be taken of the state of the art. The facts constituting the state of the art are normally subject to the possibility of rational disagreement among reasonable men and are not amenable to the taking of such notice.").

[7] *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697. While the court explained that, "as an administrative tribunal the Board clearly has expertise in the subject matter over which it exercises jurisdiction," it make clear that such "expertise may provide sufficient support for conclusions [only] as to peripheral issue." *Id.* at 1385-86, 59 USPQ2d at 1697.

[8] *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697. See also *In re Lee*, __F.3d at __, 61 USPQ2d at 1435.

[9] See *In re Lee*, __F.3d at __, 61 USPQ2d 1434-35; *In re Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697 (holding that general conclusions concerning what is "basic knowledge" or "common sense" to one of ordinary skill in the art without specific factual findings and some concrete evidence in the record to support these findings will not support an obviousness rejection).

[10] See *In re Soli*, 317 F.2d 941, 945-46, 137 USPQ 797, 800 (CCPA 1963) (the court accepted the examiner's assertion that the use of "a control is standard procedure throughout the entire field of bacteriology" because it was readily verifiable and disclosed in references of record not cited by the Office); *In re Chevenard*, 139 F.2d 711, 713, 60 USPQ 239, 241 (CCPA 1943) (accepting examiner's finding that a brief heating at a higher temperature was the equivalent of a longer heating at a lower temperature where there was nothing in the record to indicate the contrary and where the applicant never demanded that the examiner produce evidence to support his statement).

[11] See *Soli*, 317 F.2d at 946, 37 USPQ at 801; *Chevenard*, 139 F.2d at 713, 60 USPQ at 241.

[12] See 37 CFR 1.111(b). See also *Chevenard*, 139 F.2d at 713, 60 USPQ at 241 ("[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention.").

[13] See 37 CFR 1.104(c)(2). See also *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697 ("the Board [or examiner] must point to some concrete evidence in the record in support of these findings" to satisfy the substantial evidence test).

[14] See *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697; *Ahlert*, 424 F.2d at 1092, 165 USPQ 421.

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